IN THE CLAIMS:

1. (Previously presented) A computer system comprising:

a central processing unit (CPU);

a peripheral bus;

a bus interface unit coupled to accommodate communications between said CPU and said peripheral bus;

a first daughtercard configured to assert a first configuration change signal in response to said first daughtercard being inserted within a first connector associated with said peripheral bus;

a second daughtercard configured to assert a second configuration change signal in response to said second daughtercard being inserted within a second connector associated with said peripheral bus; and

wherein said bus interface unit includes a storage unit including a first storage location for storing a state of said first configuration change signal and a second storage location for storing a state of said second configuration change signal, and wherein the first storage location is coupled to receive the first configuration change signal via a first signal line and the second storage location is coupled to receive the second configuration change signal over a second signal line that is separate from the first signal line.

2. (Original) The computer system as recited in claim 1, wherein said first configuration change signal has a first state and a second state.

3. (Original) The computer system as recited in claim 2, wherein said first state is a logic-low voltage.

4. (Original) The computer system as recited in claim 3, wherein said first state indicates that said first daughtercard has been recently inserted into said first connector.

5. (Original) The computer system as recited in claim 4, wherein said first state indicates that said first daughtercard is to be extracted from said first connector.

6. (Original) The computer system as recited in claim 1, wherein a state of said first configuration change signal is read from said storage unit on a periodic basis.

7. (Original) The computer system as recited in claim 1, wherein said peripheral bus is a peripheral component interconnect (PCI) bus.

8. (Original) The computer system as recited in claim 1, wherein said computer system is configured to drive a sense signal to said first daughtercard upon insertion of said first daughtercard into said first connector.

9. (Original) The computer system as recited in claim 8, wherein said computer system is configured to receive a presence detect signal upon insertion of said first daughtercard into said first connector.

10. (Original) The computer system as recited in claim 9, wherein said computer system is configured to drive a reset signal to said first daughtercard in response to receiving said presence detect signal.

11. (Original) The computer system as recited in claim 10, wherein said first daughtercard includes power control circuitry, wherein said power control

circuitry is configured to perform a power-up sequence on said first daughtercard in response to receiving said sense signal from said computer system.

12. (Original) The computer system as recited in claim 11, wherein said first daughtercard is configured to drive a board ok signal to said computer system following completion of said power-up sequence.

13. (Original) The computer system as recited in claim 12, wherein said computer system is configured to de-assert said reset signal in response to receiving said board ok signal from said first daughtercard.

14. (Original) The computer system as recited in claim 13, wherein said first daughtercard is configured to assert said first configuration signal in response to said computer system de-asserting said reset signal.

15. (Original) The computer system as recited in claim 14, wherein said computer system is configured to establish software communications between said computer system and said first daughtercard in response to a detection of said first configuration change signal.

16. (Original) The computer system as recited in claim 15, wherein said first configuration change signal is deasserted upon establishing software communications between said computer system and said first daughtercard.

17. (Original) The computer system as recited in claim 1, wherein said first daughtercard includes at least one ejector handle.

18. (Original) The computer system as recited in claim 17, wherein said first daughtercard includes a switch configured to be actuated by said ejector handle.

19. (Original) The computer system as recited in claim 18, wherein said first configuration change signal is asserted in response to an actuation of said switch.

20. (Original) The computer system as recited in claim 19, wherein said computer system is configured to terminate software communications between said computer system and said first daughtercard in response to an assertion of said first configuration change signal.

21. (Original) The computer system as recited in claim 20, wherein said computer system is configured to de-assert a sense signal upon termination of software communications between said computer system and said first daughtercard.

22. (Original) The computer system as recited in claim 20, wherein said computer system is configured to drive a reset signal to said first daughtercard upon termination of software communications between said computer system and said first daughtercard.

23. (Original) The computer system as recited in claim 22, wherein said first daughtercard includes a light-emitting diode (LED).

24. (Original) The computer system as recited in claim 23, wherein said LED is illuminated in response to upon termination of software communications between said computer system and said first daughtercard.

25. (Original) The computer system as recited in claim 1, wherein said first daughtercard and said second daughtercard are configured for hot swapping.

26. (Previously presented) A method for hot-swapping daughtercards in an operating computer system, the computer system comprising a central processing unit (CPU), a peripheral bus, and a bus interface unit including a storage unit, said bus

interface unit configured to accommodate communications between said CPU and said peripheral bus, the method comprising:

inserting a first daughtercard into a first connector associated with said peripheral bus;

inserting a second daughtercard into a second connector associated with said peripheral bus;

asserting a first configuration change signal, said first configuration change signal asserted by said first daughtercard;

asserting a second configuration change signal, said second configuration change signal asserted by said second daughtercard;

storing a state of said first configuration change signal in a first storage location of said storage unit, wherein the first configuration change signal is received by the first storage location via a first signal line; and

storing a state of said second configuration change signal in a second storage location of said storage unit, wherein the second configuration change signal is received by the second storage location via a second signal line, wherein the second signal line is separate from the first signal line.

27. (Original) The method as recited in claim 26, wherein said first configuration signal has a first state and a second state.

28. (Original) The method as recited in claim 27, wherein said first state is a logic-low voltage.

29. (Original) The method as recited in claim 28, wherein said first state indicates that said first daughtercard has been recently inserted into said first connector.

30. (Original) The method as recited in claim 28, wherein said first state indicates that said first daughtercard is to be extracted from said first connector.

31. (Original) The method as recited in claim 26, wherein a state of said first configuration change signal is read from said storage unit on a periodic basis.

32. (Original) The method as recited in claim 26, wherein said peripheral bus is a peripheral component interconnect (PCI) bus.

33. (Original) The method as recited in claim 26, wherein said computer system is configured to drive a sense signal to said first daughtercard upon insertion of said first daughtercard into said first connector.

34. (Original) The method as recited in claim 33, wherein said computer system is configured to receive a presence detect signal upon insertion of said first daughtercard into said first connector.

35. (Original) The method as recited in claim 34, wherein said computer system is configured to drive a reset signal to said first daughtercard in response to receiving said presence detect signal.

36. (Original) The method as recited in claim 35, wherein said first daughtercard includes power control circuitry, wherein said power control circuitry is configured to perform a power-up sequence on said first daughtercard in response to receiving said sense signal from said computer system.

37. (Original) The method as recited in claim 36, wherein said first daughtercard is configured to drive a board ok signal to said computer system following completion of said power-up sequence.

38. (Original) The method as recited in claim 37, wherein said computer system is configured to de-assert said reset signal in response to receiving said board ok signal from said first daughtercard.

39. (Original) The method as recited in claim 38, wherein said first daughtercard is configured to assert said first configuration change signal in response to said computer system de-asserting said reset signal.

40. (Original) The method as recited in claim 39, wherein said computer system is configured to establish software communications between said computer system and said first daughtercard in response to a detection of said first configuration change signal.

41. (Original) The method as recited in claim 40, wherein said first configuration change signal is de-asserted upon establishing software communications between said computer system and said first daughtercard.

42. (Original) The method as recited in claim 26, wherein said first configuration change signal is asserted in response to actuation of a switch mounted to said first daughtercard, wherein said switch is configured to be actuated by an ejector handle.

43. (Original) The method as recited in claim 42, wherein said computer system is configured to terminate software communications between said computer system and said first daughtercard in response to an assertion of said first configuration change signal.

44. (Original) The method as recited in claim 43, wherein said computer system is configured to de-assert a sense signal upon termination of software communications between said computer system and said first daughtercard.

45. (Original) The method as recited in claim 44, wherein said computer system is configured to drive a reset signal to said first daughtercard in response to termination of software communications between said computer system and said first daughtercard.

46. (Original) The method as recited in claim 44, wherein said first daughtercard is configured to illuminate a light-emitting diode (LED) in response to termination of software communications between said computer system and said first daughtercard.